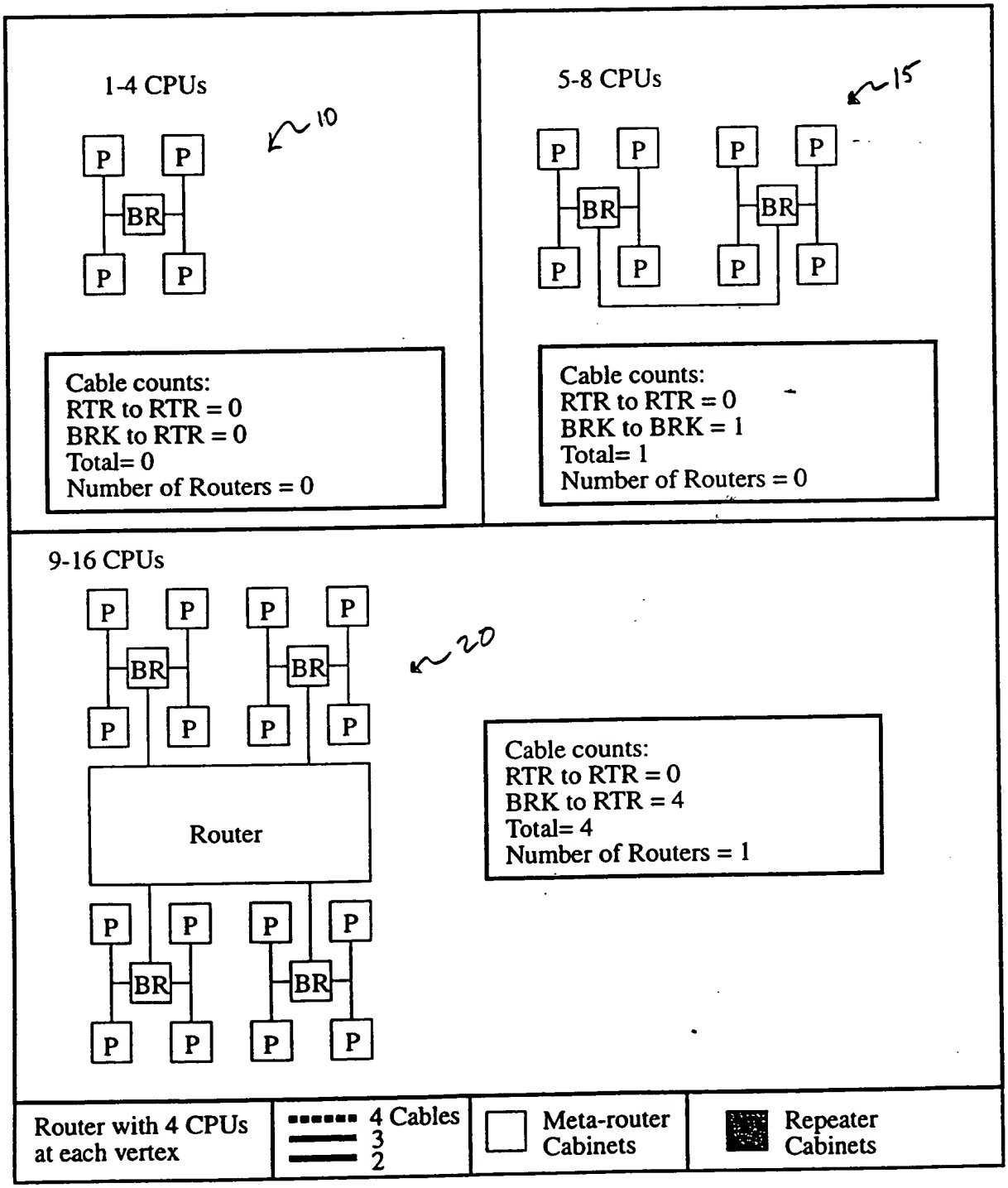
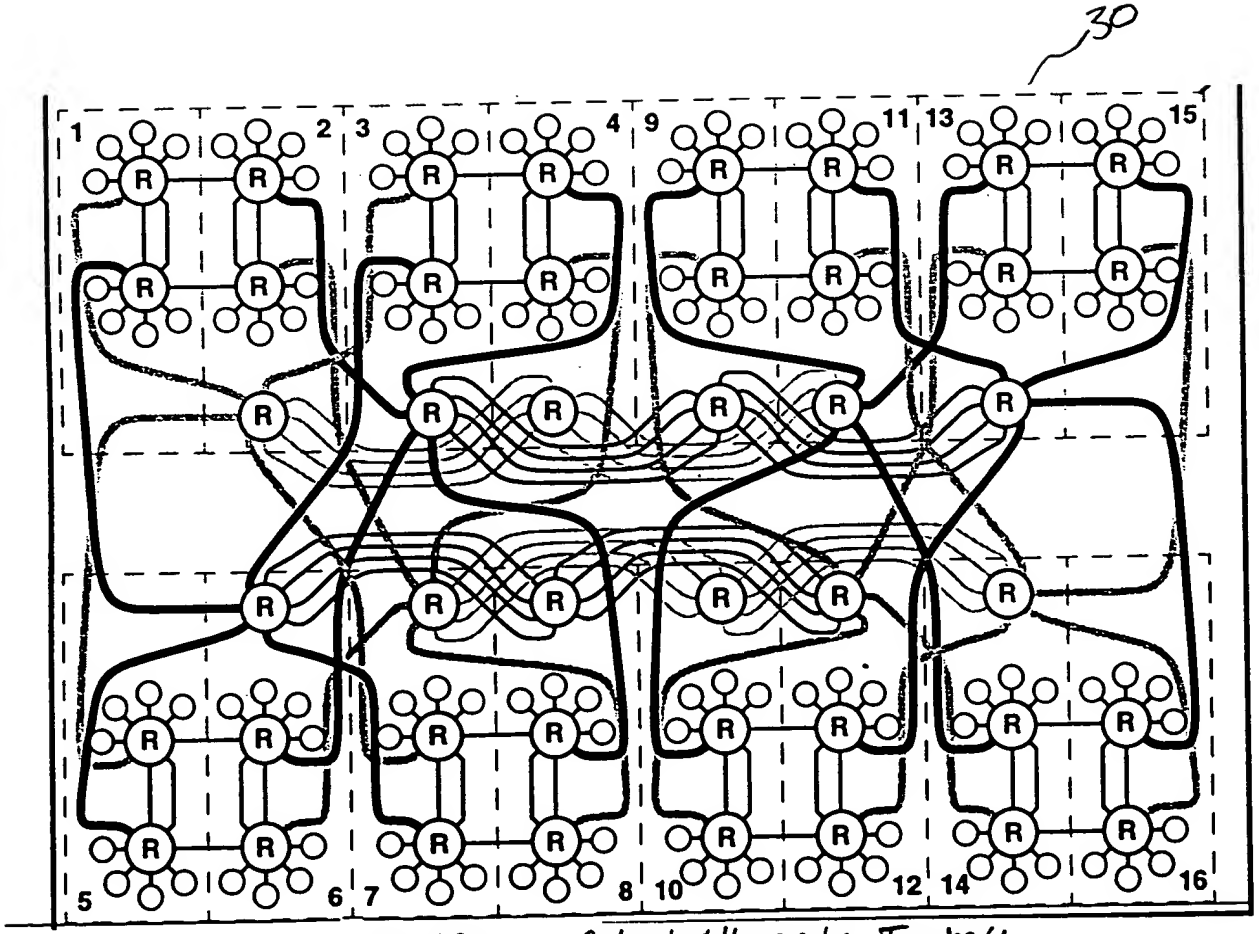
FIG 1A


1-4 CPUs
10
P
BR
Cable counts:
RTR to RTR = 0
BRK to RTR = 0
Total= 0
Number of Routers = 0
5-8 CPUs
15
Cable counts:
RTR to RTR = 0
BRK to BRK = 1
Total= 1
Number of Routers = 0
9-16 CPUs
20
Router
Cable counts:
RTR to RTR = 0
BRK to RTR = 4
Total= 4
Number of Routers = 1
Router with 4 CPUs at each vertex
4 Cables
3
2
Meta-router Cabinets
Repeater Cabinets




512 CPU Extended Hypercube Topology

FIG 1B

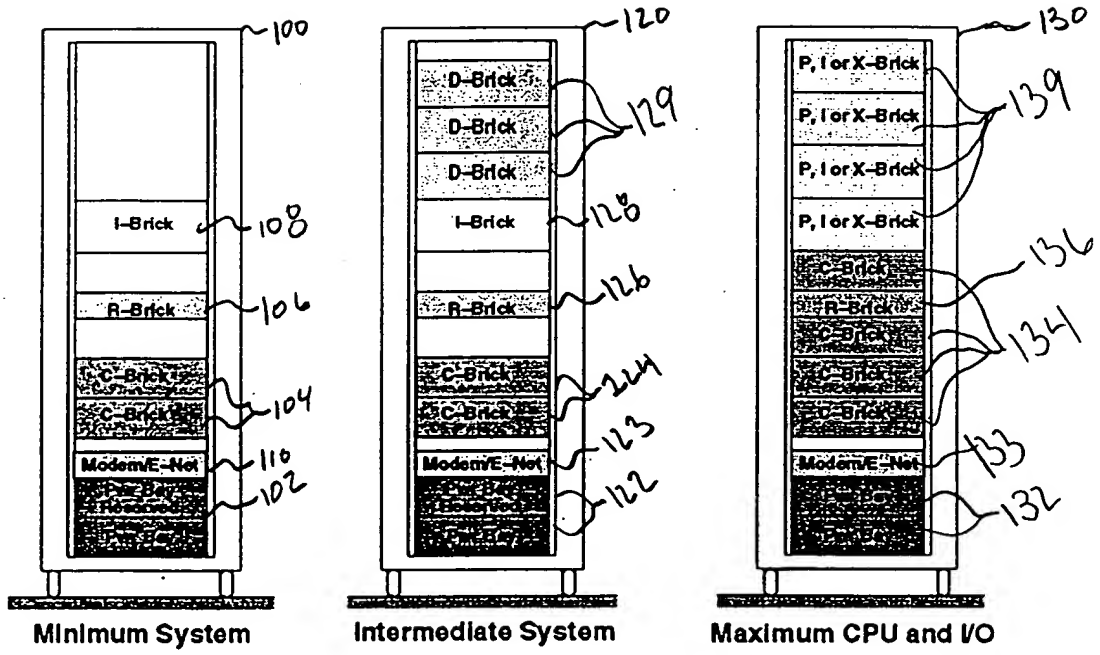
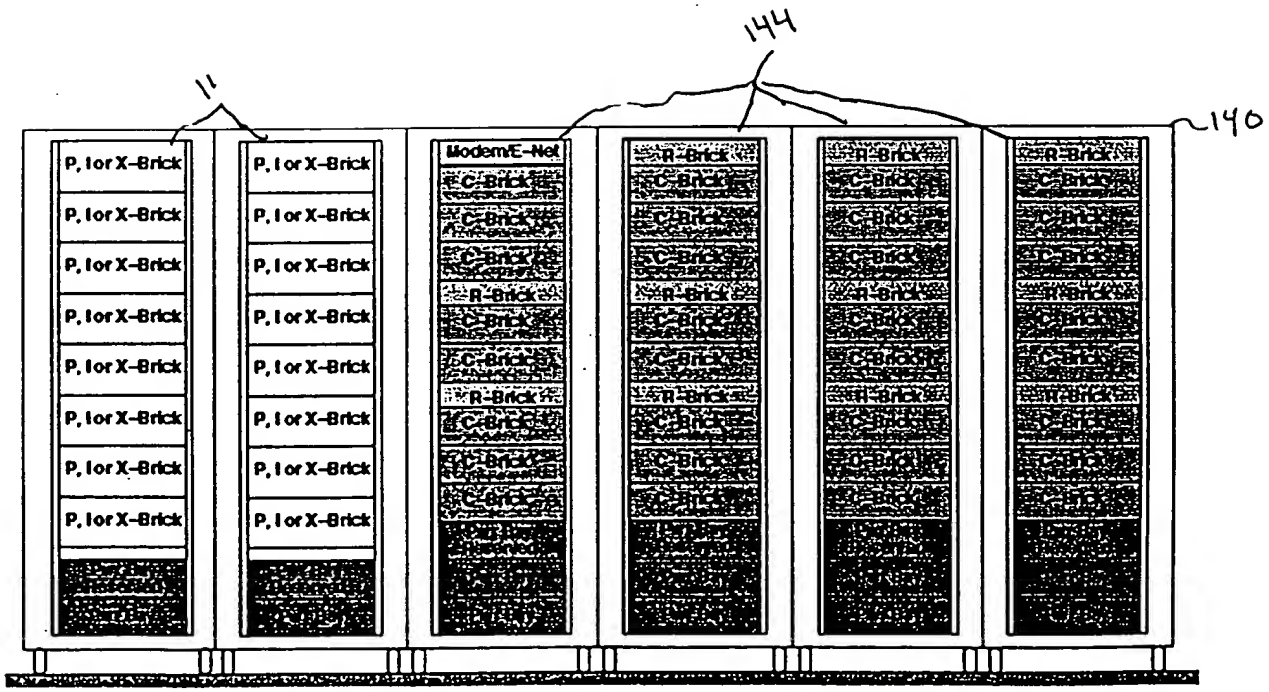

100
I-Brick
108
R-Brick
106
C-Brick
C-Brick
104
Modem/E-Net
110
102
Minimum System
120
D-Brick
D-Brick
D-Brick
129
I-Brick
128
R-Brick
126
C-Brick
C-Brick
124
Modem/E-Net
123
122
Intermediate System
130
P, I or X-Brick
P, I or X-Brick
P, I or X-Brick
P, I or X-Brick
139
C-Brick
R-Brick
C-Brick
C-Brick
C-Brick
136
134
Modem/E-Net
133
132
Maximum CPU and I/O

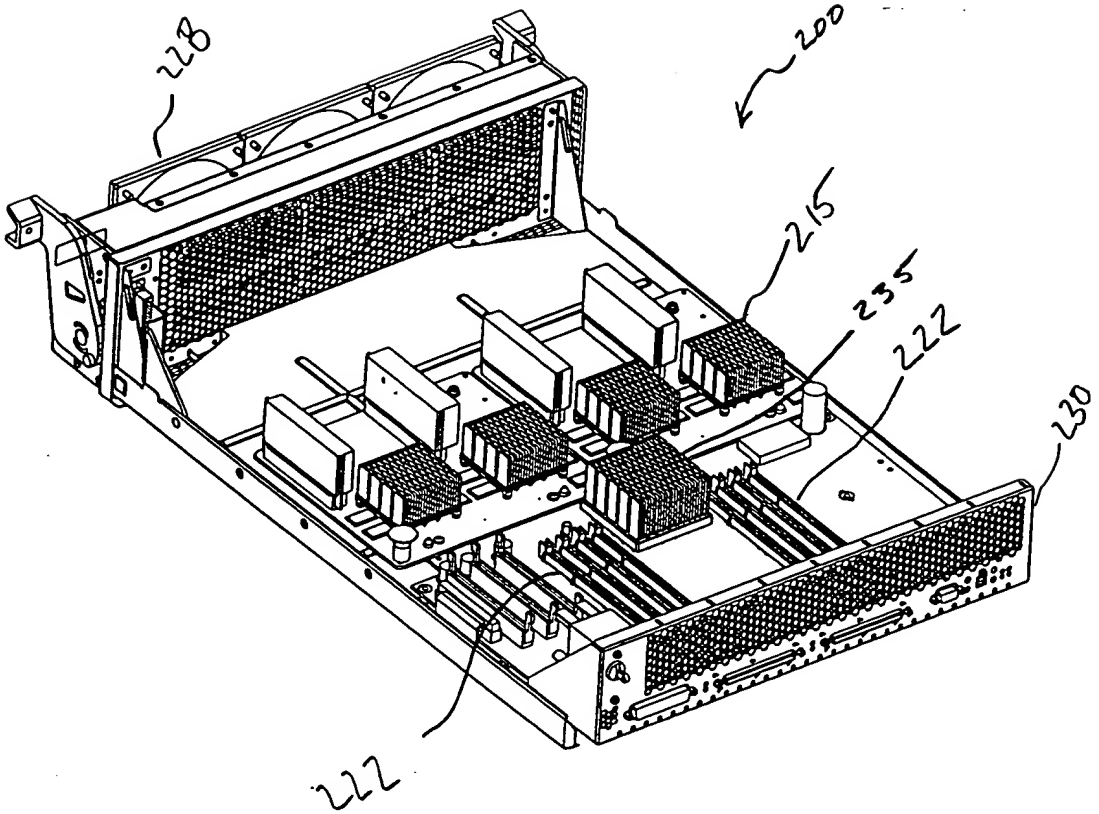
FIG. 1C




Quadrant of 512P Single System Image

FIG 1D

FIG 2A



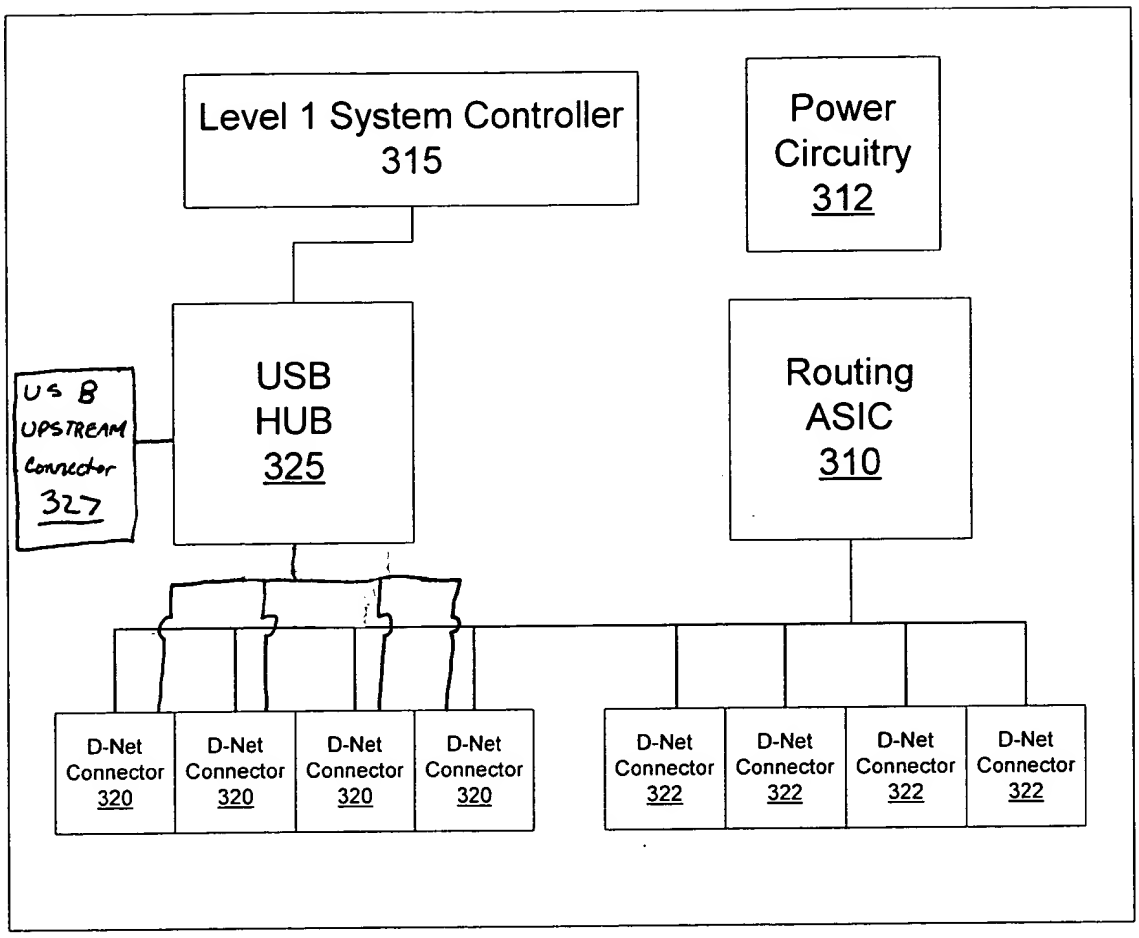

Level 1 System Controller
315
Power
Circuitry
312
USB
HUB
325
Routing
ASIC
310
USB
UPSTREAM
Connector
327
D-Net
Connector
320
D-Net
Connector
320
D-Net
Connector
320
D-Net
Connector
320
D-Net
Connector
322
D-Net
Connector
322
D-Net
Connector
322
D-Net
Connector
322

Figure 3

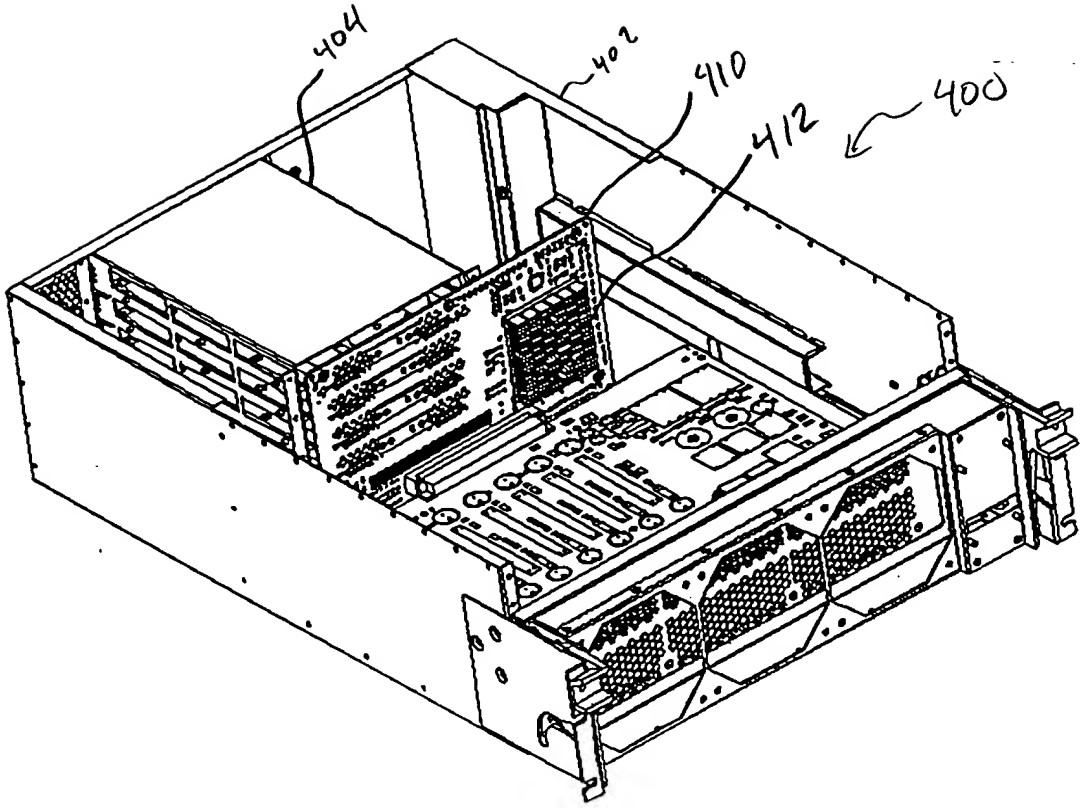
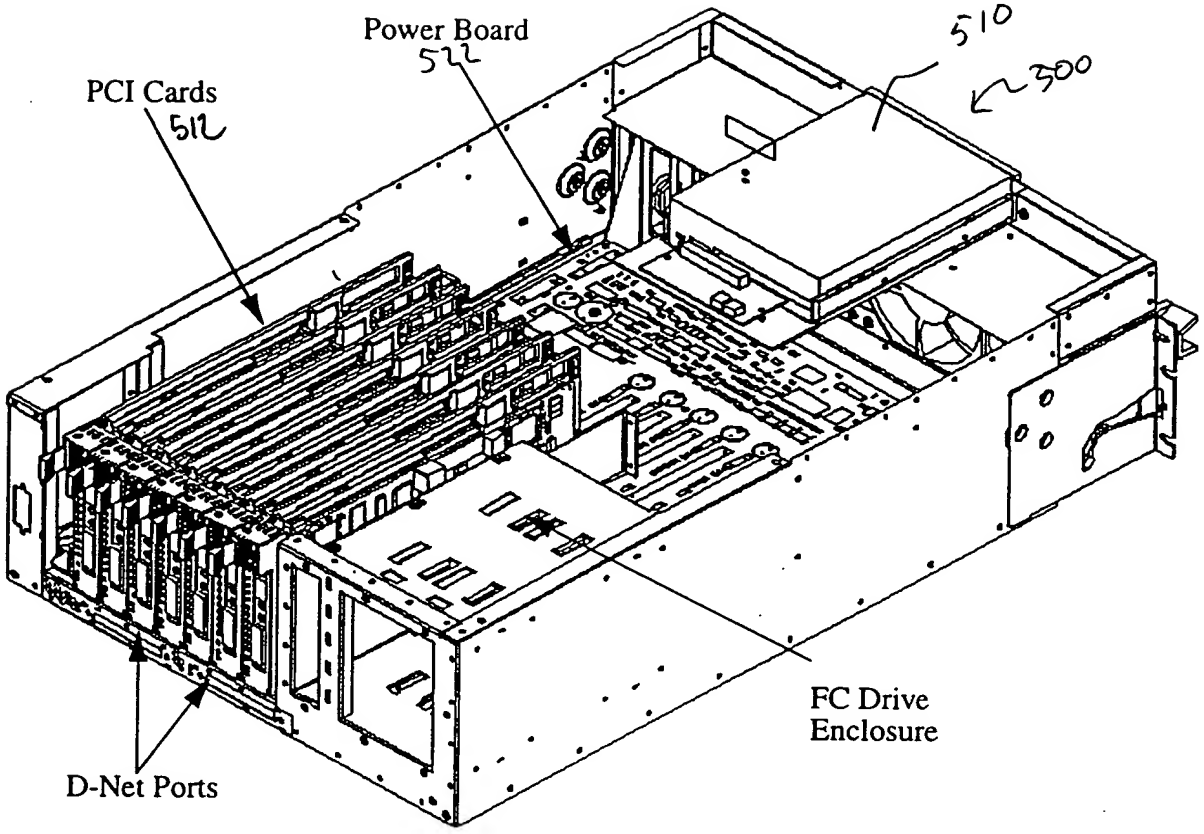



FIG. 4

FIG 5


Power Board
522
PCI Cards
512
510
300
FC Drive
Enclosure
D-Net Ports

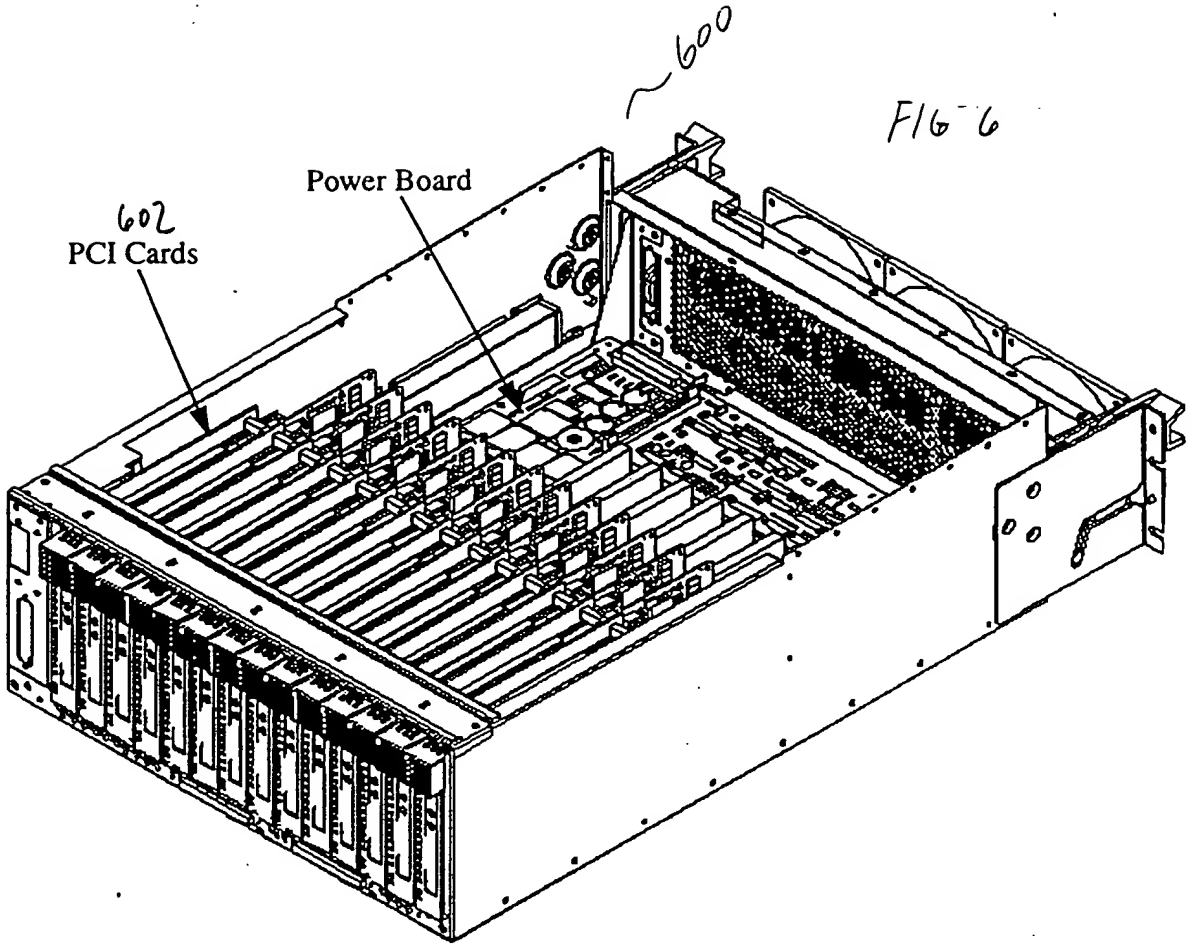



FIG 6

FIG. 7

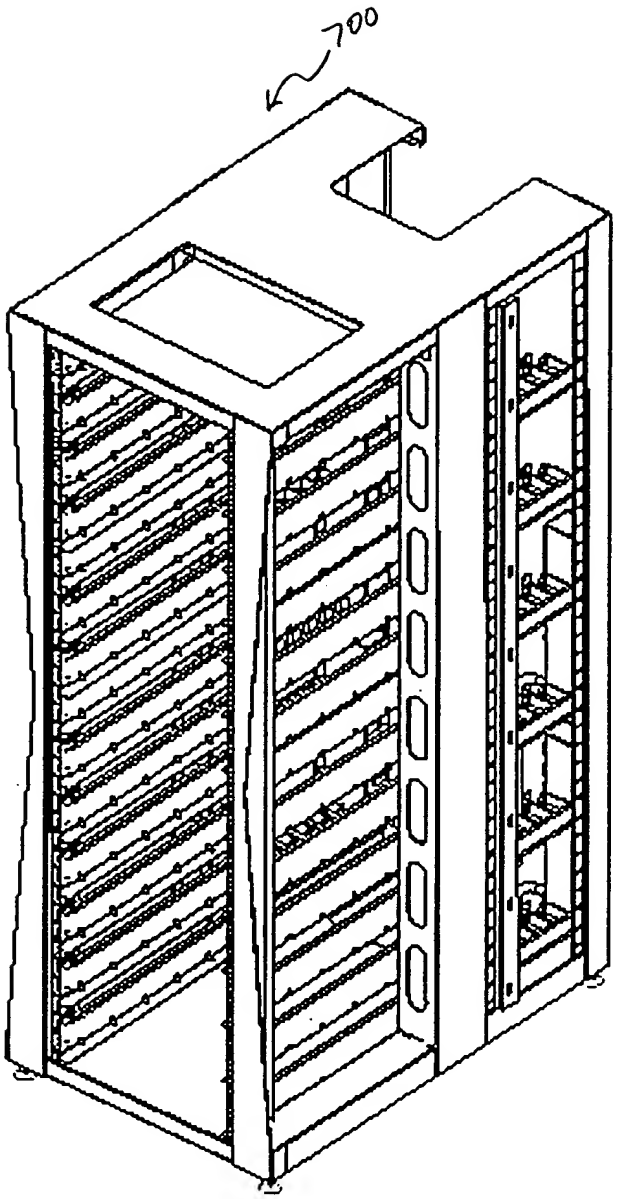


FIG 8

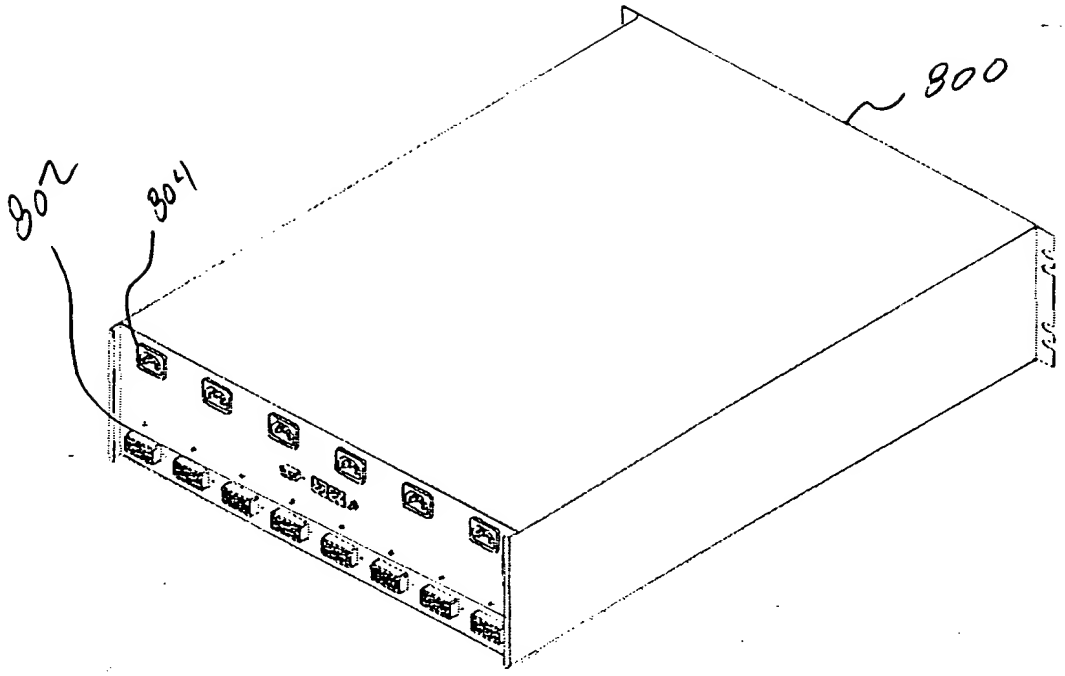
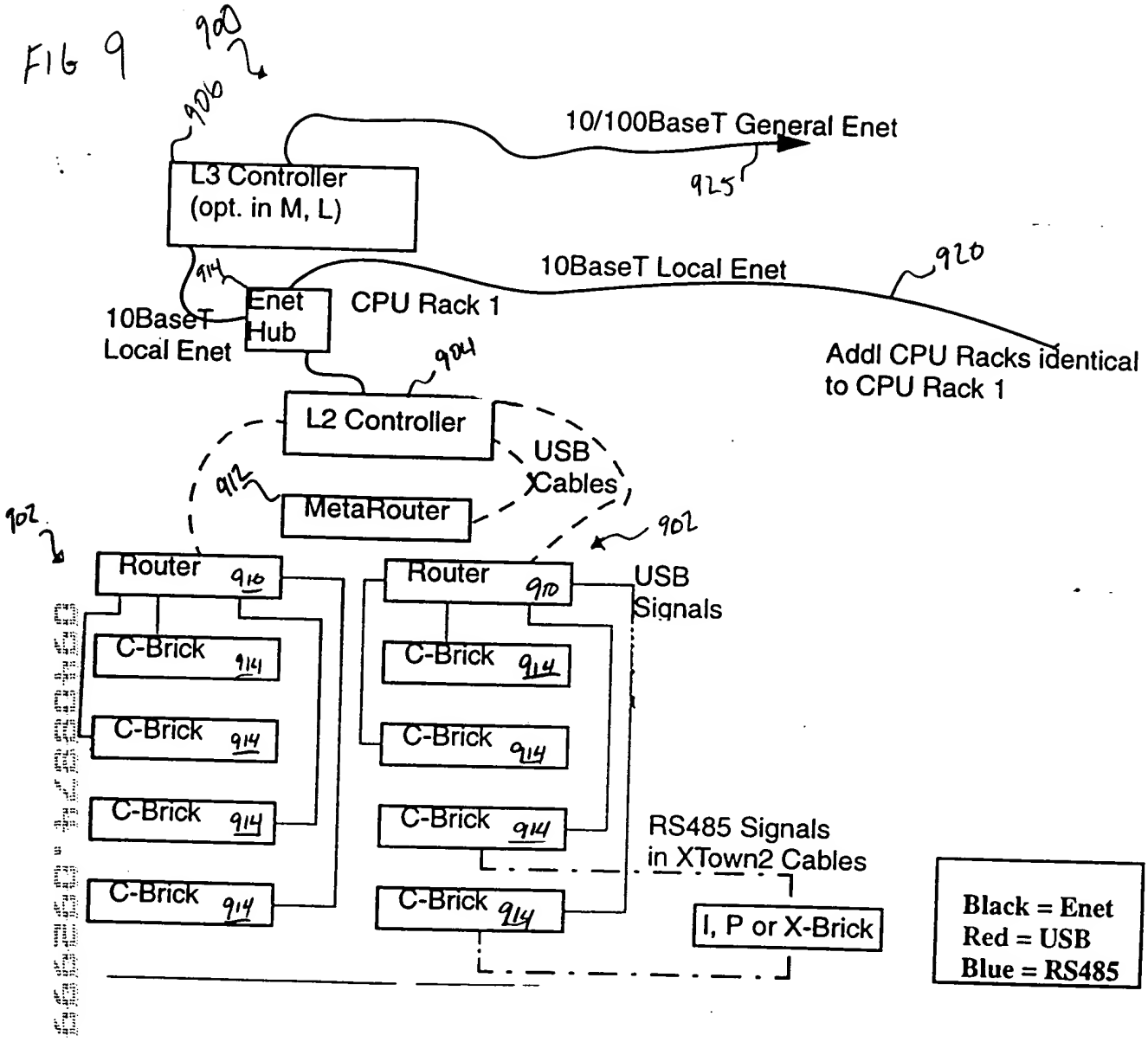


FIG 9


900
906
L3 Controller
(opt. in M, L)
10/100BaseT General Enet
925
914
Enet
Hub
10BaseT
Local Enet
CPU Rack 1
10BaseT Local Enet
920
Addl CPU Racks identical
to CPU Rack 1
904
L2 Controller
USB
Cables
912
MetaRouter
902
902
Router
910
Router
910
USB
Signals
C-Brick
914
C-Brick
914
C-Brick
914
C-Brick
914
C-Brick
914
C-Brick
914
C-Brick
914
C-Brick
914
RS485 Signals
in XTown2 Cables
I, P or X-Brick
Black = Enet
Red = USB
Blue = RS485

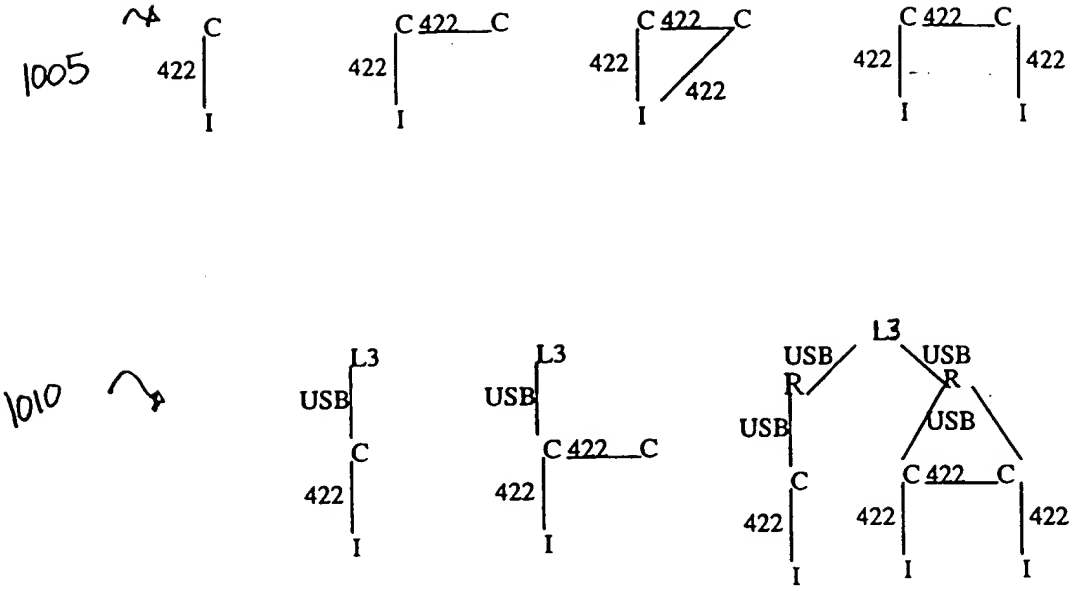

1005
C
422
I
C 422 C
422
I
C 422 C
422
422
I
C 422 C
422
422
I
1010
L3
USB
C
422
I
L3
USB
C 422 C
422
I
L3
USB
R
USB
C
422
I
USB
R
USB
C 422 C
422
422
I

FIG 10

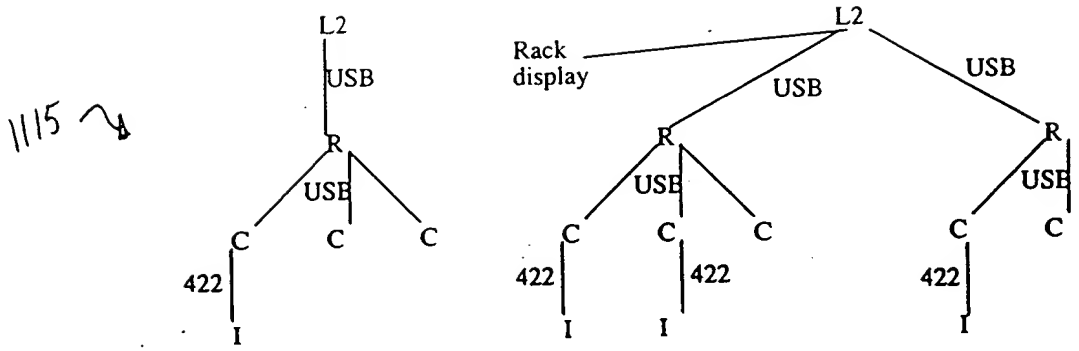

1115
L2
USB
R
USB
C
C
C
422
I
L2
Rack
display
USB
USB
R
R
USB
USB
C
C
C
C
C
422
422
422
I
I
I

FIG. 11

FIG 12

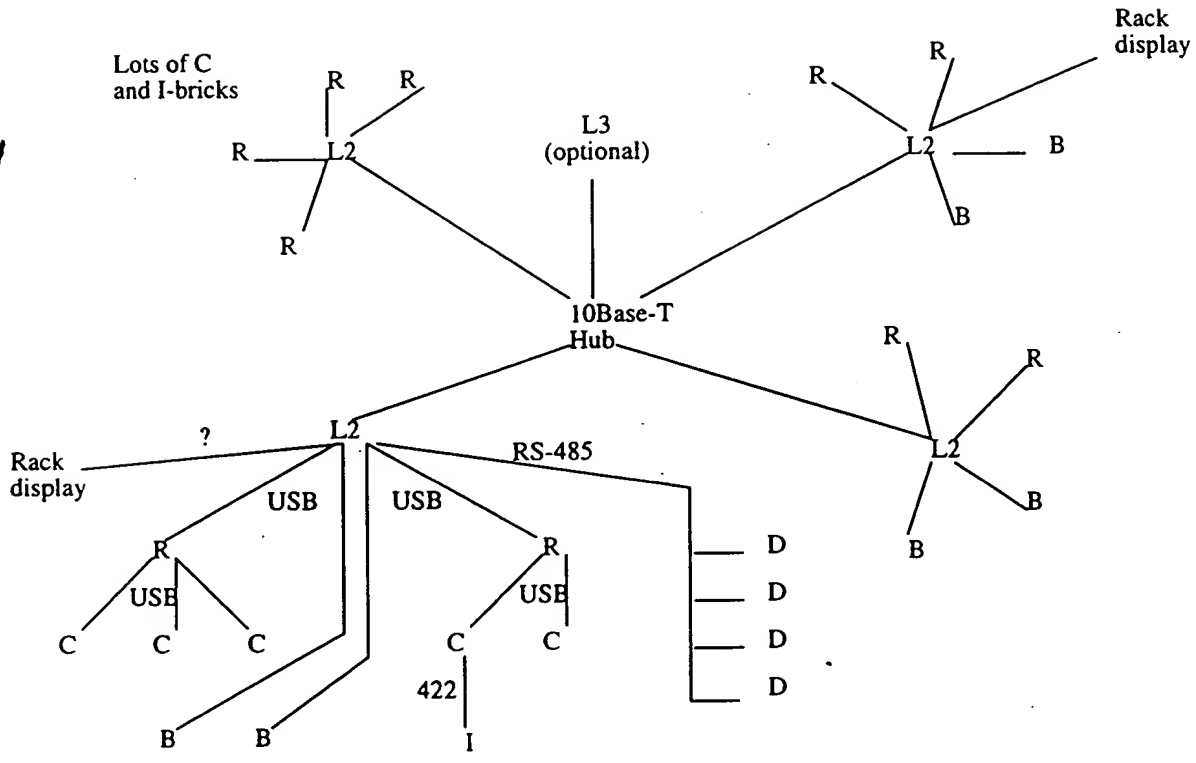

208
Lots of C
and I-bricks
R
R
R
L2
R
L3
(optional)
R
R
L2
B
B
Rack
display
10Base-T
Hub
R
R
L2
B
B
?
L2
Rack
display
USB
USB
RS-485
R
USB
C
C
C
B
B
R
USB
C
C
422
I
D
D
D
D

FIG. 13

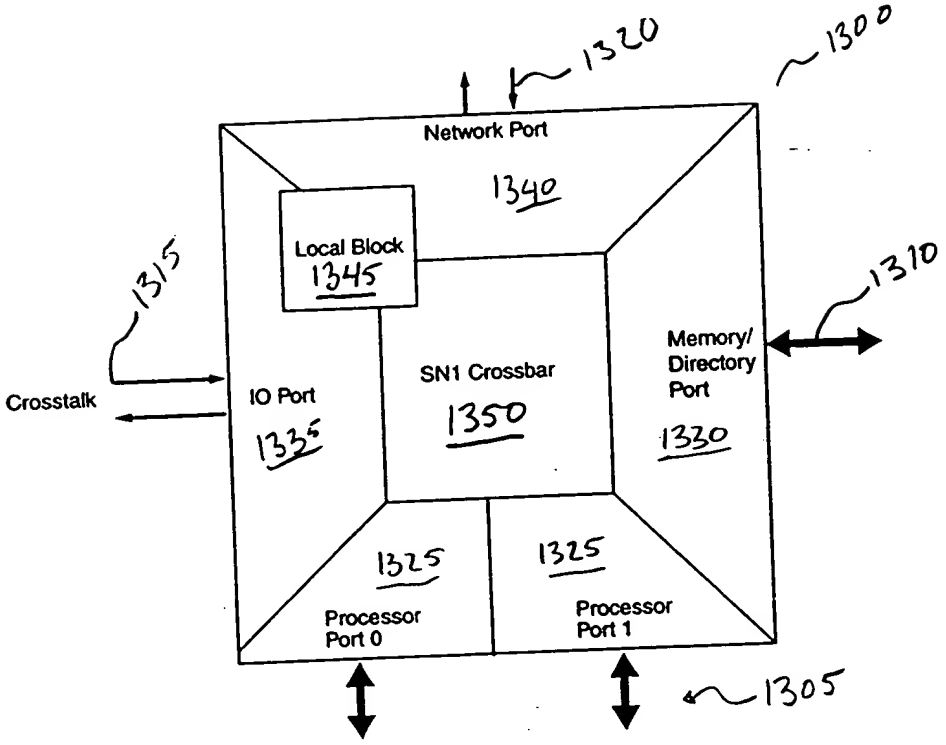
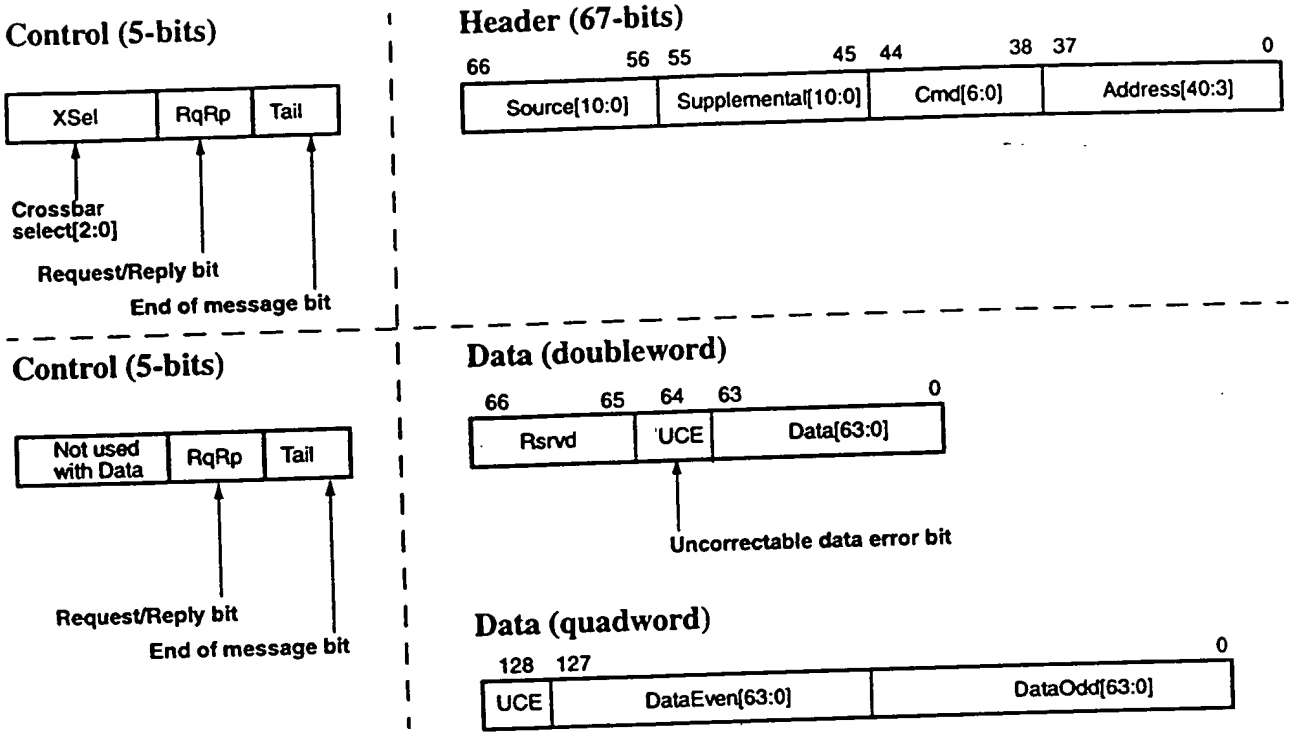
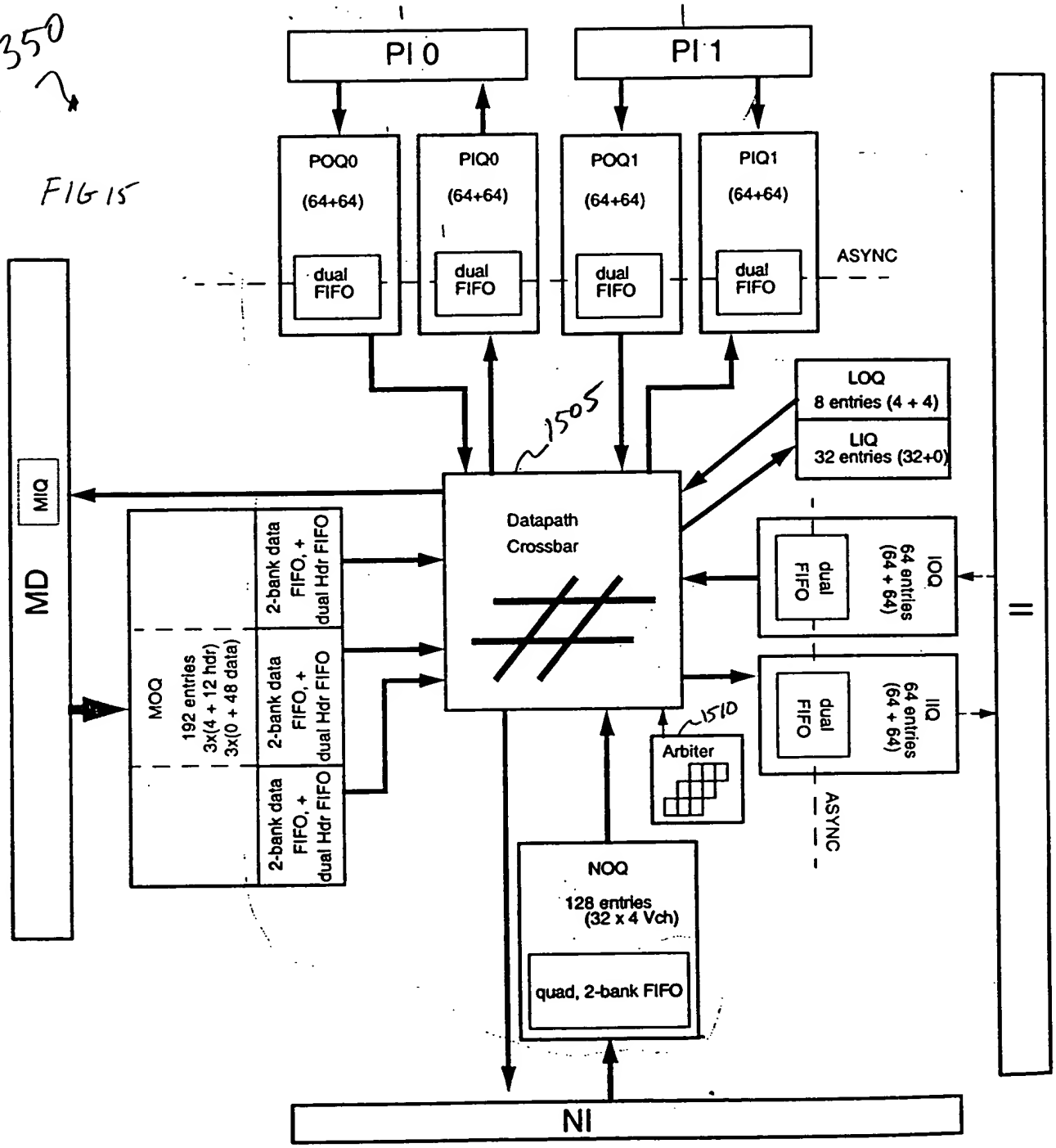

1320
1300
Network Port
1340
Local Block
1345
1315
1310
Crosstalk
IO Port
1335
SN1 Crossbar
1350
Memory/
Directory
Port
1330
1325
1325
Processor
Port 0
Processor
Port 1
1305

FIG 14


Control (5-bits)
XSel
RqRp
Tail
Crossbar select[2:0]
Request/Reply bit
End of message bit
Header (67-bits)
66
56
55
45
44
38
37
0
Source[10:0]
Supplemental[10:0]
Cmd[6:0]
Address[40:3]
Control (5-bits)
Not used with Data
RqRp
Tail
Request/Reply bit
End of message bit
Data (doubleword)
66
65
64
63
0
Rsrvd
UCE
Data[63:0]
Uncorrectable data error bit
Data (quadword)
128
127
0
UCE
DataEven[63:0]
DataOdd[63:0]

1350

FIG 15


PI 0
PI 1
POQ0
(64+64)
PIQ0
(64+64)
POQ1
(64+64)
PIQ1
(64+64)
dual FIFO
ASYNC
LOQ
8 entries (4 + 4)
LIQ
32 entries (32+0)
1505
MD
MIQ
MOQ
192 entries
3x(4 + 12 hdr)
3x(0 + 48 data)
2-bank data FIFO, + dual Hdr FIFO
Datapath
Crossbar
IOQ
64 entries
(64 + 64)
IIQ
64 entries
(64 + 64)
1510
Arbiter
NOQ
128 entries
(32 x 4 Vch)
quad, 2-bank FIFO
II
NI